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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/722,432	11/28/2003	Young Hoon Kwark	YOR920030378US1	7371

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EXAMINER	
BEVERIDGE, RACHEL E	

ART UNIT	PAPER NUMBER
1725	

DATE MAILED: 03/15/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/722,432	KWARK ET AL.	
	Examiner	Art Unit	
	Rachel E. Beveridge	1725	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 November 2003*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) *25 and 26* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,5,7-15,19,20,23,24,27,29 and 30* is/are rejected.

7)☒ Claim(s) *4, 6, 16, 18, 21, 22, and 28* is/are objected to.

8)☒ Claim(s) *1-30* are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

Applicant's election with traverse of claims 25 and 26 in the reply filed on November 11, 2005 is acknowledged. The traversal is on the ground(s) that product claim 25 has a similar description, as claimed, as method claim 1. This is not found persuasive because a search of Group II would require a search in class/subclass, 438/26, which is not required for a search of Group I.

The requirement is still deemed proper and is therefore made FINAL.

This application contains claims 25 and 26 drawn to an invention nonelected with traverse in paper dated February 22, 2006. A complete reply to the final rejection must include cancellation of nonelected claims or other appropriate action (37 CFR 1.144) See MPEP § 821.01.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-3, 5, 7, 9, 12, 14, 19, 24, and 27-29 are rejected under 35 U.S.C. 102(b) as being anticipated by Horiuchi et al. (US 6,084,295).

With respect to claim 1, Horiuchi discloses electrically connecting a semiconductor chip (10) to a connection (12) on a circuit board (5) (column 5, lines 51-

54). Horiuchi teaches a plurality of bonding wires (20) with conductive wire and electro-insulation coating for electrically connecting the circuit board (5) to the semiconductor chip (10) (column 2, lines 1-9). Horiuchi also discloses matching the impedance to that of a signal line by selecting the insulation material (column 5, lines 29-33).

With regard to claim 2, Horiuchi further teaches predetermined distances between each wire and shows wires subsequently above each other in figure 1.

Regarding claim 3, Horiuchi also shows wires in a predetermined configuration alongside one another in figures 7(a) and 8.

Regarding claim 5, Horiuchi discloses "it is possible to make the impedance-matching as a signal line by the selection of material (dielectric constant) and/or thickness of the resin coating *32* covering the conductive wire" (column 5, lines 29-33).

With respect to claim 7, Horiuchi teaches the resin coating (32) to cover the bonding section and an electro-conductive resin (34) used for shielding (column 6, lines 14-17). Figure 3 also shows an epoxy type coating (30) on a gold wire (28) to be the bond wire (20) connecting the signal between semiconductor and circuit board.

With respect to claim 9, Horiuchi also shows wires in a predetermined configuration alongside one another in figures 7(a) and 8.

With regard to claim 12, Horiuchi's figure 3 shows a round bonding wire.

With regard to claim 14, the examiner interpreted the claim to be a combination of only round wires. Horiuchi's figure 3 shows a round bonding wire.

Regarding claim 19, the examiner interpreted high to be any value for dielectric constant of the insulating material due to the lack of relation to a low value and lack of

specified values for a high dielectric constant. Horiuchi discloses matching the impedance to that of a signal line by selecting the insulation material (column 5, lines 29-33) and that an electro-conductive resin (34) is capable of easily shielding the semiconductor chip (10) (column 5, lines 34-37). Horiuchi also discloses the lack of risk of a short-circuit between the bonding wires (20) even though they are shielded with electro-conductive resin (34) because the electrode terminals and bonding section between the wires (20) and pads (22) are covered with electro-insulation resin (32) (column 5, lines 37-44).

With respect to claim 24, Horiuchi discloses electrically connecting a semiconductor chip (10) to a connection (12) on a circuit board (5) (column 5, lines 51-54). Horiuchi teaches a plurality of bonding wires (20) with conductive wire and electro-insulation coating for electrically connecting the circuit board (5) to the semiconductor chip (10) (column 2, lines 1-9). Horiuchi also discloses matching the impedance to that of a signal line by selecting the insulation material (column 5, lines 29-33).

Regarding claim 27, Horiuchi discloses electrically connecting a semiconductor chip (10) to a connection (12) on a circuit board (5) (column 5, lines 51-54). Horiuchi teaches a plurality of bonding wires (20) with conductive wire and electro-insulation coating for electrically connecting the circuit board (5) to the semiconductor chip (10) (column 2, lines 1-9). Horiuchi also discloses matching the impedance to that of a signal line by selecting the insulation material (column 5, lines 29-33). Horiuchi further teaches predetermined distances between each wire and shows wires subsequently above each other in figure 1.

With regard to claim 29, Horiuchi discloses "it is possible to make the impedance-matching as a signal line by the selection of material (dielectric constant) and/or thickness of the resin coating *32* covering the conductive wire" (column 5, lines 29-33). Figures 8 and 9 clearly show a predetermined pattern and distance between the wires (42) with dielectric material (40) surrounding them. Horiuchi also teaches carefully selecting the dielectric material for the dielectric constant "and/or" thickness (column 5, lines 34-37).

Claim 23 is rejected under 35 U.S.C. 102(b) as being anticipated by Notani et al. (US 5,294,897).

Notani discloses the reduction of the reflection of high frequency signals caused by the mismatching of characteristic impedances in the transmission line (column 6, lines 6-9). Notani also discloses a transmission line with continuous transmission between the lines and the circuit package substrate (column 5, lines 34-40). Furthermore, Notani shows a plurality of bonding wires in figures 1(a), 4(b), 6, 7, 8, and 10.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Horiuchi et al. (US 6,084,295) as applied to claim 5 above, and further in view of Chia et al. (US 2004/0182911 A1).

Horiuchi teaches epoxy as insulation but lacks disclosure of the type of epoxy used for the invention. Chia teaches wire bonding utilizing an insulating liquid (112), more specifically using ultra-violet light-cured epoxies (Chia et al., page 1, paragraph [0021], lines 3-4). Therefore, it would have been obvious to one of ordinary skill the art at the time of the invention to modify the wire bonding method of Horiuchi to utilize the ultra-violet light-cured epoxy of Chia in order to electrically insulate the bonding wires and attach them to the package in any desired sequence without causing package defects (Chia et al., page 2, paragraph [0026], lines 3-7).

Claims 10-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Horiuchi et al. (US 6,084,295) as applied to claim 1 above, and further in view of Steranko et al. (US 3,840,169).

With respect to claim 10, Horiuchi teaches dispensing wires for bonding but lacks disclosure of co-dispensing a plurality of bonding wires. However, Steranko discloses bonding multiple wires to a circuit board continuously (abstract, lines 1-9) as shown in figure 1. Regarding claim 11, Horiuchi discloses "it is possible to make the impedance-matching as a signal line by the selection of material (dielectric constant) and/or thickness of the resin coating *32* covering the conductive wire" (column 5, lines 29-33). Figures 8 and 9 clearly show a predetermined pattern and distance between the wires

(42) with dielectric material (40) surrounding them. Horiuchi also teaches carefully selecting the dielectric material for the dielectric constant "and/or" thickness (column 5, lines 34-37). However, Horiuchi lacks disclosure of co-dispensing a plurality of bonding wires. Steranko discloses bonding multiple wires to a circuit board continuously (abstract, lines 1-9) as shown in figure 1. It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the wire bonding method of Horiuchi to include the co-dispensing apparatus of Steranko in order to have strong bonding of multiple wires at one time (Steranko et al., column 1, lines 40-44).

Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Horiuchi et al. (US 6,084,295) as applied to claim 1 above, and further in view of Lee (US 2001/00154900 A1).

Horiuchi discloses bonding a plurality of bonding wires for signal transmission between and semiconductor chip (10) and a circuit board (5). However, Horiuchi lacks bonding a plurality of ribbon wires in the package. Lee teaches ribbon bonding wire for signal transmission (page 3, paragraph [0031], lines 3-10). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the wire bonding method of Horiuchi to include the bonding of ribbon bonding wire between the chip and circuit board in order to model transverse distribution adequately and utilize a wire-grid method to understand the influence of material during signal transmission (Lee, page 3, paragraph [0031], lines 6-10, and paragraph [0030}, lines 4-6).

Claims 15 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Horiuchi et al. (US 6,084,295) as applied to claim 1 above, and further in view of Notani et al. (US 5, 924,897).

With respect to claim 15, Horiuchi lacks specific description of the bonding wires to comprise a microstrip. Notani discloses a transmission line having a microstrip line structure (column 7, lines 1-2). Regarding claim 17, it is understood that a microstrip transmits a single-ended signal as disclosed by the applicant. Therefore, Notani's disclosure of a transmission line having a microstrip structure (column 7, lines 1-2) satisfies a single-ended signal. It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the wire bonding method of Horiuchi to include the disclosed microstrip of Notani in order to arrange the strip signal conductor opposite a ground conductor on the dielectric (Notani et al., column 7, lines 2-3).

Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Horiuchi et al. (US 6,084,295) as applied to claim 19 above, and further in view of Kurtz et al. (US 4,555,052).

The examiner interpreted high to be any value for dielectric constant of the insulating material due to the lack of relation to a low value and lack of specified values for a high dielectric constant. Horiuchi lacks disclosure of the particular material comprising the dielectric. However, Kurtz discloses ceramic as a dielectric material useful for electric insulation (column 6, lines 52-57). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the wire

bonding method of Horiuchi to include the ceramic dielectric of Kurtz in order to properly bond the wire for transmission while the package is grounded (Kurtz et al., column 6, lines 47-52).

Claim 30 is rejected under 35 U.S.C. 103(a) as being unpatentable over Horiuchi et al. (US 6,084,295) as applied to claim 28 above, and further in view of Notani et al. (US 5,294,897).

Horiuchi lacks specific description of the bonding wires to comprise a microstrip. Notani discloses a transmission line having a microstrip line structure (column 7, lines 1-2). It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the wire bonding method of Horiuchi to include the disclosed microstrip of Notani in order to arrange the strip signal conductor opposite a ground conductor on the dielectric (Notani et al., column 7, lines 2-3).

Allowable Subject Matter

Claims 4,6, 16, 18, 21, and 22 are objected to but would be allowable if the independent claim 1 and dependent claim 5 were allowable.

Regarding claim 4, prior art set the conductive resin at ground potential but does not set the bond wire at ground potential.

Regarding claim 6, prior art shows continuous dielectric material surrounding bonding wires; however, the periodic placement of dielectric material around bonding

wires was not found in prior art and is therefore in condition for allowance if the independent claim 1 and dependent claim 5 were allowable.

Regarding claim 16, no prior art was found disclosing a plurality of bonding wires for signal transmission comprising a coplanar waveguide or similar structure fitting the applicant's definition of coplanar waveguide. Therefore, the claim is in condition for allowance if the independent claim 1 was allowable.

Regarding claim 18, no prior art was found disclosing a differential signal via a plurality of bonding wires. Therefore, the claim is in condition for allowance if the independent claim 1 was allowable.

Regarding claim 21, prior art discusses impedance matching but lacks applicants claim of a filter where a particular response is being tailored and impedance transformer which seeks to match different impedances on the respective termini.

Regarding claim 22, prior art was found to show effect of an impedance transformer (see discussion of claim 21); however, due to the claims dependence on claim 6, no prior art was found to include the effect with respect to the periodic placement of dielectric material around bonding wires. Thus, the claim is in condition for allowance if the independent claim 1 and dependent claims 5-6 were allowable.

Claim 28 is objected to but would be allowable if the independent claim 27 was allowable.

Prior art discloses connections between semiconductor chip and circuit board but not imply or suggest that the impedances of the connection must be matched.

Response to Arguments

With respect to claims 1-3, 5, 7-15, 17, 19-20, 23-24, 27, and 29-30, applicant's arguments filed February 22, 2006 have been fully considered but they are not persuasive.

With respect to claim 1, in the lengthy argument on pages 12 and 13 of applicants traversal applicant argues "there are elements of the claimed invention that are not taught or suggest by Horiuchi, and, since the rejection currently of record relies upon primary reference Horiuchi for all pending claims, all claims are clearly patentable over Horiuchi" (p.13). The examiner points the applicant to Horiuchi's teaching of bonding wires (20) operating as a coaxial cable line, and his statement that "it is also possible to make the impedance-matching as a signal line by the selection of material (dielectric constant) and /or thickness of the resin coating 32 covering the conductive wire" (Horiuchi, col. 5, lines 28-33). Horiuchi also discloses improvement of the electrical characteristics of the device for signals transmitted through the bonding wires (20). The examiner points out that "wires" implies multiple wires, which includes applicant's claim of 2 bonding wires. Further, Horiuchi discloses a signal line and the effects on its impedance by choice of a material for the bonding wires. Applicant does not specify why his wires provide a controlled impedance effect (in claim 1), and thus there is no distinction between the claimed wires and Horiuchi's disclosure. The applicant states, Horiuchi fails to satisfy the plain meaning of the claim language, since a grounded electroconductive resin, rather than a second bonding wire, is used to

provide the impedance matching (p.12). The examiner agrees that the resin "covering the conductive wire" (Horiuchi, col. 5, line 33) is the reason for the impedance effects in Horiuchi, the claim language does not encompass applicant's argument that "the second bonding wire" is causing the controlled impedance effect. The claim merely says, "configured" to provide the controlled impedance effect, and the examiner notes that "configured" can encompass both applicant's second wire and Horiuchi's resin for controlling the impedance effects of the signal line.

Regarding claim 2, applicant argues the configuration of the wires according to the claim language is not anticipated by Horiuchi (p.13). The examiner disagrees. Although the applicant claims a more specific configuration in claim 2, applicant does not specify that the newly claimed configuration of claim 2 is creating the controlled impedance effect. Furthermore, the examiner understands that Horiuchi teaches the effects of a resin around the bonding wires to provide for the impedance effect in his invention. However, Horiuchi's configuration in figure 1 is sufficient to anticipate the applicant's claim of "predetermined distances." Further definition or more specific definition of the actual distance might be sufficient to deem the claim allowable; however, as stated currently, "predetermined distances" can include any distance including no distance, as appears to be the configuration in Horiuchi's figure 1. Applicant also admits, "Horiuchi shows wires in a predetermined configuration" (p.14). The examiner further notes that, during patent examination, the pending claims must be "given the broadest reasonable interpretation." Applicant always has the opportunity to amend the claims during prosecution, and broad interpretation by the examiner reduces

the possibility that the claim, once issued, will be interpreted more broadly than is justified. In re Prater, 415 F.2d 1393, 1404-05, 162 USPQ 541, 550-51 (CCPA 1969).

Applicant argues that "the separations shown in Figure 7a, 7b, and 8 when compared to the diameter of the wires would be ineffective in providing any controlled impedance effect" with respect to claim 3 (p.13). The examiner neither agrees nor disagrees with applicant. The argument is extraneous to the broad claim, which merely states a "predetermined distance" separates the first and second bonding wires. Horiuchi's figures clearly anticipate this requirement.

In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., "formulas required for the exemplary microstrip and/or coplanar waveguide configurations as outlined in the present invention" in regard to claim 5 on p.14) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Applicant argues claim 7 is allowable relating back to arguments from claims 1 and 5. The examiner disagrees and points applicant to the responses previously stated.

With regard to claim 8, applicant argues, applicants submit the use of UV-cured epoxy involved in several embodiments of the present invention is novel, even if the element is already know in the art, since the rejection demonstrates that it is not known in the combination of elements described by the claim (p.14). The examiner disagrees and directs the applicant to the rejection and response to arguments for claim 1.

Horiuchi clearly anticipates claim 1 and therefore is sufficient to obviously combine with the UV-cured epoxy of Chia.

Applicant argues Horiuchi's invention "is an entirely different concept from that of the present invention and reinforces the observation that this method is only done to meet the mechanical requirements of the package, not to provide any impedance control function, since it is unlikely that the two spacings will coincide" (p.14). Applicant further says, "Horiuchi makes no suggestion to use more than one wire for a signal line" (p. 14). The examiner disagrees. The examiner points the applicant to Horiuchi's teaching of bonding wires (20) operating as a coaxial cable line, and his statement that "it is also possible to make the impedance-matching as a signal line by the selection of material (dielectric constant) and /or thickness of the resin coating 32 covering the conductive wire" (Horiuchi, col. 5, lines 28-33). Horiuchi also discloses improvement of the electrical characteristics of the device for signals transmitted through the bonding wires (20). The examiner points out that "wires" implies multiple wires, which includes applicant's claim of 3 bonding wires.

In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., simultaneous bonding of wirebonds in the extremely close proximities that the present invention operates, with reference to claims 10 and 11 on p.15) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993). Furthermore, the new drawings supplied

in arguments were not originally submitted with the application and have no patentable weight on the claim language.

Applicant argues with respect to claims 12 and 14, that although "Horiuchi's figure 3 shows a round bonding wire" the round bonding wire fails to overcome the deficiency of claim 1 (p.15). The examiner disagrees with reference to the rejection and response to claim 1 previously discussed.

In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., ribbon bonding wires where only "one wire is used per electrode," with regard to claim 13 on p.15) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

With reference to claims 15 and 17, applicant argues that Notani's invention is "a well known planar microstrip configuration" (p.15). Therefore, applicant has admitted Notani discloses a microstrip and the examiner maintains obviousness to combine with the invention of Horiuchi with dependence on broad claim 1. Furthermore, in response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., bond wires which are usually suspended in air or embedded in epoxy for the return current function which may be ground, p.15-16) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read

into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Applicant argues Horiuchi in isolation fails to overcome the deficiency for claim 1. The examiner disagrees and directs the applicant to the rejection and response to arguments over claim 1.

Regarding claim 20, applicant states, "merely identifying ceramic as an electric insulation fails to satisfy the plain meaning of the claim language, as one having ordinary skill in the art would interpret this claim in conjunction with its antecedent claims" (p.16). Again, the examiner disagrees and directs the applicant to the rejection and response to arguments over claim 1.

With respect to claim 23, applicant argues Notani's disclosure of a plurality of bonding wires that are both connected to the same electrode and the reduction of parasitic effects requires additional components to achieve this effect (p.16). The examiner understands Nontani's invention and reminds the applicant that the argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., implied bonding wires connected to separate electrodes, p.16) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Applicant argues Horiuchi fails to overcome the deficiencies identified for the parent claim with regard to claims 24 and 27 (p.16). The examiner points out that

claims 24 and 27 and independent of any parent claims and are rejected by Horiuchi on their own merits.

The applicant argues that figures 8 and 9 of Horiuchi refer to the substrate geometry and not to the bond wire and are therefore irrelevant to claim 29 (p.17). Although the examine agrees that Horiuchi's figures 8 and 9 refer to the substrate geometry, the examine disagrees that they are irrelevant to claim 29. Furthermore, Horiuchi discloses the bonding wires (20) connected to the conductive vias (42), which are shown in these figures) (Horiuchi, col. 7, lines 15-28). Therefore, it is apparent that the via structure on the substrate shown in figures 8 and 9 corresponds with the wire structures, since they are attached at those points, and Horiuchi therefore anticipates the applicants claim.

Applicant argues in reference to claim 30 that Notani's invention extends a planar microstrip geometry (p.17). Again the examiner notes that the applicant has admitted Notani discloses a microstrip and the examiner maintains obviousness to combine with the invention of Horiuchi. Furthermore, in response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., wirebond carrying the ground (return) current) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

In response to applicant's argument that there is no suggestion to combine the references (p.17), the examiner recognizes that obviousness can only be established by

combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988) and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, see Chia et al., [0026], lines 3-7; Steranko et al., column 1, lines 40-44; Lee, page 3, [0030], lines 4-6); Notani et al., column 7, lines 2-3; and Kurtz et al., column 6, lines 47-52.

Applicant's arguments, see pages 14, 16, and 17, filed February 22, 2006, with respect to claims 4, 21, and 28 have been fully considered and are persuasive. The rejections of claims 14, 16, and 17 have been withdrawn.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Rachel E. Beveridge whose telephone number is 571-272-5169. The examiner can normally be reached on Monday through Friday, 9 am to 6 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Patrick Ryan can be reached on 571-272-1292. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JONATHAN JOHNSON
PRIMARY EXAMINER

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